Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-25 (Canceled)

26. (New) A semiconductor device comprising:

a first insulating layer;

a first lower interconnection and a second lower interconnection formed in the first insulating layer;

a capping layer formed over the first insulating layer and having first and second windows respectively exposing the first and second lower interconnections; and,

a first metal resistor extending along the capping layer and contacting respective top surfaces of the first and second lower interconnections through the respective first and second windows;

wherein the first metal resistor is not contacted from above by any electrical contact or interconnection.

27. (New) The device of claim 26, wherein the first metal resistor is formed of a material selected from a group consisting of titanium, titanium nitride, tantalum, tantalum nitride, and tantalum silicon nitride.

28. (New) The device of claim 27, wherein the first metal resistor has a thickness of about 30 Å to 1000 Å.

29. (New) The device of claim 26, wherein the capping layer is formed of a material selected from a group consisting of silicon nitride and silicon carbide.

30. (New) The device of claim 26, wherein the first metal resistor includes a series of undulations or bends.

31. (New) The device of claim 26, wherein the first metal resistor has a linear shape.

32. (New) The device of claim 26, further comprising:

a third lower interconnection formed in the first insulating layer;

a second insulating layer formed on the capping layer and the first metal resistor;

an upper interconnection formed on the second insulating layer and connected to the third lower interconnection via a contact.

33. (New) The device of claim 26, further comprising:

a third lower interconnection formed in the first insulating layer; and,

an upper electrode formed on the capping layer above the third lower interconnection.

34. (New) The device of claim 26, further comprising:

a lower electrode formed on the capping layer;

a dielectric layer formed on the lower electrode; and,

an upper electrode formed on the dielectric layer above the lower electrode;

wherein the lower electrode, the dielectric layer, and the upper electrode form a metal-insulator-metal (MIM) capacitor.

35. (New) The device of claim 26, further comprising:

third, fourth, and fifth lower interconnections each formed in the first insulating layer;

a third window formed in the capping layer to expose the third lower interconnection;

a lower electrode formed on the capping layer above the third lower interconnection and contacting the third lower interconnection through the third window;

a dielectric layer formed on the capping layer over the first metal resistor and the lower electrode;

an upper electrode formed on the dielectric layer over the lower electrode;

fourth and fifth windows penetrating the dielectric layer and the capping layer to expose the respective fourth and fifth lower interconnections; and,

a second metal resistor extending along the dielectric layer and contacting the fourth and fifth lower interconnections through the respective fourth and fifth windows.

36. (New) The device of claim 35, further comprising:

a second insulating layer formed on the dielectric layer over the upper electrode and the second metal resistor;

a sixth lower interconnection formed in the first insulating layer;

a contact formed through the second insulating layer, the dielectric, and the capping layer to contact the sixth lower interconnection; and,

an upper interconnection formed on the second insulating layer and contacting the contact.

37. (New) A semiconductor device, comprising:

a first insulating layer;

first, second, and third lower interconnections formed in the first insulating layer;

a first window formed in the capping layer to expose the first lower interconnection;

a lower electrode formed on the capping layer and contacting the first lower interconnection through the first window;

a dielectric layer formed on the capping layer over the lower electrode;

second and third windows penetrating the dielectric layer and the capping layer to expose the respective second and third lower interconnections; and,

a metal resistor extending along the dielectric layer and contacting the second and third lower interconnections through the second and third windows.

38. (New) The device of claim 37, further comprising:

a fourth lower interconnection formed in the first insulating layer;

a second insulating layer formed on the dielectric layer above the metal resistor and the upper electrode;

a contact formed through the second insulating layer, the dielectric, and the capping layer to contact the fourth lower interconnection; and,

an upper interconnection formed on the second insulating layer and contacting the contact.

39. (New) The device of claim 37, wherein the metal resistor is formed of a material selected from a group consisting of titanium, titanium nitride, tantalum, tantalum nitride, and tantalum silicon nitride.

40. (New) A semiconductor device, comprising:

a first insulating layer;

a second insulating layer;

first and second lower interconnections formed in the first insulating layer;

a first etch stop layer formed on the first insulating layer;

first and second windows formed in the first etch stop layer to expose the respective first and second lower interconnections;

first and second contacts formed in respective first and second contact holes extending through the second insulating layer, the first and second contacts respectively contacting the first and second lower interconnections through the first and second windows;

a metal resistor extending along the second insulating layer and contacting the first and second contacts;

a second etch stop layer formed on the second insulating layer and over the metal resistor;

a third lower interconnection formed in the first insulating layer;

a third window formed in the first etch stop layer to expose the third lower interconnection;

a third contact formed in a third contact hole extending through the second insulating layer, the third contact contacting the third lower interconnection through the third window; and,

an upper interconnection formed on the second insulating layer and contacting the third contact.

41. (New) The device of claim 40, wherein the metal resistor is formed of a material selected from a group consisting of titanium, titanium nitride, tantalum, tantalum nitride, and tantalum silicon nitride.